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CLAIMS:

1. A method of fabricating integrated circuitry comprising:

forming a conductive line having opposing sidewalls over a semiconductor substrate;

depositing an insulating layer over the substrate and the line;

etching the insulating layer proximate the line along at least a portion of at least one sidewall of the line; and

after the etching, depositing an insulating spacer forming layer over the substrate and the line, and anisotropically etching it to form an insulating sidewall spacer along said portion of the at least one sidewall.

2. The method of claim 1 wherein the etching of the insulating layer is conducted along at least a portion of each of the opposing line sidewalls, the anisotropic etching forming an insulating sidewall spacer over each of the opposing line sidewalls.

3. The method of claim 1 wherein the etching of the insulating layer is conducted along the portion of the one sidewall and not along the opposing sidewall.

4. The method of claim 1 wherein the portion comprises a majority of said one sidewall.

5. The method of claim 1 wherein the portion comprises the substantial entirety of said at least one sidewall.

6. The method of claim 1 wherein the etching of the insulating layer outwardly exposes material of the semiconductor substrate.

7. The method of claim 1 wherein the conductive line is formed to comprise a transistor gate.

8. The method of claim 1 comprising planarizing the insulating layer prior to said etching of it.

9. The method of claim 1 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with one of the active area regions.

10. A method of fabricating integrated circuitry comprising:

forming a pair of transistor gates having respective opposing sidewalls over a semiconductor substrate, one sidewall of one of the transistor gates facing one sidewall of the other transistor gate;

depositing an insulating layer over the substrate and between the pair of transistor gates to fill an area extending therebetween;

etching a contact opening into the insulating layer to proximate the substrate between the pair of transistor gates;

depositing an insulating spacer forming layer within the contact opening to less than completely fill the contact opening; and

anisotropically etching the spacer forming layer to form a pair of insulating sidewall spacers over the one sidewalls of the pair of transistor gates.

11. The method of claim 10 wherein the contact opening etching exposes material of the semiconductor substrate.

12. The method of claim 10 wherein the contact opening etching exposes conductive material of at least one of the pair of transistor gates.

13. The method of claim 10 wherein the contact opening etching exposes conductive material of each of the pair of transistor gates.

14. The method of claim 10 wherein the contact opening etching exposes conductive material of at least one of the sidewalls of at least one of the pair of transistor gates.

15. The method of claim 10 comprising planarizing the insulating layer prior to said etching of it.

16. The method of claim 10 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with one of the active area regions.

17. A method of fabricating integrated circuitry comprising:

forming a pair of transistor gates having respective opposing sidewalls over a semiconductor substrate, one sidewall of one of the transistor gates facing one sidewall of the other transistor gate;

depositing an insulating layer over the substrate and between the pair of transistor gates to fill an area extending therebetween;

etching a contact opening into the insulating layer to proximate the substrate between the pair of transistor gates, the etching exposing conductive material of at least one of the one sidewalls of the pair of transistor gates;

after the etching, covering the at least one of the one sidewalls with insulating material; and

forming electrically conductive material within the opening in electrical connection with material of the semiconductor substrate.

18. The method of claim 17 wherein the contact opening etching exposes conductive material of each of the one sidewalls of each of the pair of transistor gates.

19. The method of claim 17 wherein the covering comprises deposition of an insulating layer.

20. The method of claim 17 wherein the covering comprises deposition of an insulating layer, and subsequent anisotropic etching thereof.

21. The method of claim 17 comprising planarizing the insulating layer prior to the contact opening etching.

22. The method of claim 17 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with one of the active area regions.

23. A method of forming a local interconnect comprising:

forming a pair of transistor gates having respective opposing sidewalls over a semiconductor substrate;

depositing an insulating layer over the substrate and between the pair of transistor gates;

etching a first contact opening into the insulating layer to proximate the substrate between the pair of transistor gates and another contact opening through the insulating layer to proximate the substrate proximate an opposing side of one of the pair of transistor gates;

forming insulating sidewall spacers over the opposing sidewalls of the one transistor gate, the insulating layer being received between at least one of said sidewalls and one of said sidewall spacers; and

forming a local interconnect layer to overlie the one transistor gate and electrically connect with semiconductor substrate material between the pair of transistor gates and semiconductor substrate material proximate the opposing side of the one transistor gate.

24. The method of claim 23 wherein the insulating layer is not received between the other sidewall and the other sidewall spacer.

25. The method of claim 23 wherein the etching exposes material of the semiconductor substrate within the first and another contact openings.

26. The method of claim 23 comprising planarizing the insulating layer prior to said etching of it.

27. The method of claim 23 wherein the insulating layer as received between the one sidewall and the one sidewall spacer has a maximum lateral thickness which is greater than or equal to a maximum lateral thickness of the one sidewall spacer.

28. The method of claim 23 wherein the local interconnect layer comprises polysilicon.

29. The method of claim 23 comprising:

forming field isolation material regions and active area regions on the semiconductor substrate before the depositing;

etching a trench into the field isolation material and the insulating layer into a desired local interconnect line configuration; and

forming the local interconnect layer to at least partially fill the trench and which electrically connects with one of the active area regions.

30. A method of forming a conductive line comprising:

forming conductive material received over a semiconductor substrate into a line, the line having opposing sidewalls;

depositing insulative material over the line and etching it to be received over one of the opposing sidewalls and not the other;

depositing an insulating spacer forming layer over the line and the etched insulative material; and

anisotropically etching the spacer forming layer to form a pair of insulative spacers over the opposing line sidewalls, the insulative material being received between the one sidewall and one insulative spacer formed thereover and not being received between the other sidewall and the other spacer formed thereover.

31. The method of claim 30 comprising planarizing the insulating layer prior to said etching of it.

32. The method of claim 30 wherein the insulative material as received between the one sidewall and the one sidewall spacer formed thereover has a maximum lateral thickness which is greater than or equal to a maximum lateral thickness of the one sidewall spacer.

33. A method of forming a conductive line comprising:

forming conductive material received over a semiconductor substrate into a line, the line having opposing sidewalls;

depositing insulative material over the line;

planarizing the insulative material;

depositing an insulating spacer forming layer over the line and the planarized insulative material; and

anisotropically etching the spacer forming layer to form a pair of insulative spacers over the opposing line sidewalls, the insulative material being received between at least one of the sidewalls and one insulative spacer formed thereover.

34. The method of claim 33 wherein the insulative material as received between the one sidewall and the one sidewall spacer formed thereover has a maximum lateral thickness which is greater than or equal to a maximum lateral thickness of the one sidewall spacer.

35. A method of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates;

implanting conductivity enhancing impurity into the local interconnect layer in at least two implanting steps, one of the two implantings providing a peak implant location which is deeper into the layer than the other; and

diffusing conductivity enhancing impurity from the local interconnect layer into semiconductor substrate material therebeneath.

36. The method of claim 35 comprising conducting the one implanting relative to one portion of the local interconnect layer to have a peak implant location which is through said layer and within the semiconductor substrate material therebeneath.

37. A method of forming a local interconnect comprising:

forming at least two transistor gates over a semiconductor substrate;

depositing a local interconnect layer to overlie at least one of the transistor gates and interconnect at least one source/drain region of one of the gates with semiconductor substrate material proximate another of the transistor gates; and

implanting conductivity enhancing impurity through the local interconnect layer into semiconductor substrate material therebeneath.

38. The method of claim 37 further comprising in another implanting step separate from said implanting, implanting conductivity enhancing impurity to a peak concentration location which is within he local interconnect layer.

39. A method of fabricating integrated circuitry comprising:

forming a gate dielectric layer over a semiconductor substrate;

forming a conductively doped semiconductive layer over the gate dielectric layer;

forming an insulative capping layer over the semiconductive layer;

forming an etch stop layer over the insulative capping layer;

patterning and etching the etch stop layer, the capping layer and the semiconductive layer into a plurality of transistor gate lines;

depositing an oxide layer over the substrate and the transistor gate lines to a thickness greater than that of the combined etched etch stop layer, capping layer and semiconductor layer;

chemical mechanical polishing the deposited oxide layer using the etch stop layer as an etch stop;

patterning and etching the polished oxide layer to expose material of the semiconductor substrate in at least two discrete locations proximate different of the plurality of gate lines;

depositing a local interconnect layer into electrical connection with said locations and over said plurality of gate lines; and

etching the local interconnect layer into a local interconnect line overlying at least two of said plurality of gate lines.

40. A method of forming a conductive line comprising:

forming field isolation material regions and active area regions on a semiconductor substrate;

etching a trench into the field isolation material into a desired line configuration; and

depositing a conductive material to at least partially fill the trench and form a conductive line therein.

41. The method of claim 40 comprising forming the field isolation material to comprise LOCOS oxide.

42. The method of claim 40 comprising depositing an insulative layer over the active area and field isolation regions, and planarizing the insulative layer prior to the etching.

43. The method of claim 40 comprising depositing an insulative layer over the active area and field isolation regions, and planarizing the insulative layer prior to the etching; the etching comprising etching the trench to be received within the planarized insulative layer.

44. The method of claim 40 comprising forming the field isolation material to comprise CVD oxide formed within etched substrate trenches.

45. The method of claim 40 wherein the conductive material is initially deposited to overfill the trench, and comprising removing some of the conductive material after the initial deposition to leave the trench only partially filled with the conductive material.

46. A method of forming a local interconnect comprising:

etching a trench into field isolation material formed relative to a semiconductor substrate, the trench in the field isolation material extending to an edge of the isolation material proximate active area substrate material; and

forming a local interconnect layer of material over the substrate which at least partially fills the trench and which electrically connects with said active area substrate material.

47. The method of claim 46 comprising forming the field isolation material to comprise LOCOS oxide.

48. The method of claim 46 comprising forming the field isolation material to comprise CVD oxide formed within etched substrate trenches.

49. The method of claim 46 wherein the local interconnect layer is initially deposited to overfill the trench, and comprising removing some of the interconnect layer after the initial deposition to leave the trench only partially filled with the interconnect layer.

50. Integrated circuitry comprising:

a semiconductor substrate comprising field isolation material regions and active area regions; and

a conductive line received within a trench formed within the field isolation material.

51. The integrated circuitry of claim 50 wherein the field isolation material comprises LOCOS oxide.

52. The integrated circuitry of claim 50 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

53. The integrated circuitry of claim 50 wherein the conductive line within the trench is defined by the shape of the trench formed within the field isolation material.

54. The integrated circuitry of claim 53 wherein the field isolation material comprises LOCOS oxide.

55. The integrated circuitry of claim 53 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

56. The integrated circuitry of claim 50 wherein the trench has opposing insulative sidewalls comprising the field isolation material, conductive material of the line contacting the trench sidewalls.

57. Integrated circuitry comprising:

a semiconductor substrate comprising field isolation material regions and active area regions; and

a local interconnect line extending from over and in electrical connection with an active area region to within a trench formed within the field isolation material.

58. The integrated circuitry of claim 57 wherein the field isolation material comprises LOCOS oxide.

59. The integrated circuitry of claim 57 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

60. The integrated circuitry of claim 57 wherein the conductive line within the trench is defined by the shape of the trench formed within the field isolation material.

61. The integrated circuitry of claim 60 wherein the field isolation material comprises LOCOS oxide.

62. The integrated circuitry of claim 60 wherein the field isolation material comprises CVD oxide formed within etched substrate trenches.

63. The integrated circuitry of claim 60 wherein the trench has opposing insulative sidewalls comprising the field isolation material, conductive material of the local interconnect line contacting the trench sidewalls.